The terminology of VLIW, described in the present application, is used in a technical field of data processing architecture and does not designate a conventional VLIW architecture. In particular, a conventional VLIW architecture has an instruction group, having a plurality of conventional instructions in a data processing device. The instruction group is used as a unit in determining order of logical processing sequence. A VLIW instruction has a long bit column, being very-long-instruction word, is formed by connecting a plurality of conventional instructions having a short bit column or by connecting the plurality of conventional instructions and further adding a field or a plurality of fields. For instance, in Fig. 2a, a VLIW instruction corresponding to 101 includes bit fields of 103, 401, 404, 106, 104, 402, 405 and 107 while in Fig. 2b a VLIW instruction corresponding to 102 includes bit fields of 103, 403, 406, 108, 104, 109, 110 and hatched bit fields. In order to distinguish a VLIW instruction from a conventional instruction, the conventional instruction is called a sub-instruction in this technical field.

The same terminology "sub-instruction" is used in the description of the embodiments of the present application. However, in the claims, unlike the embodiments, to avoid a construction limited to VLIW architecture, the claims use the terminology "instruction" without using terminologies "sub-instruction" and "VLIW instruction". Thus, the Examiner seems to misunderstand that the present invention is limited to the VLIW architecture because the data processing device of a VLIW architecture is described in the embodiment of the present application.

Thus, in Fig. 2a the sub-instruction corresponds to a portion including three bit fields of 401, 404 and 106 or in Fig. 2b a portion including five bit fields of 403, 406,

Thus, in Fig. 2a the sub-instruction corresponds to a portion including three bit fields of 401, 404 and 106 or in Fig. 2b a portion including five bit fields of 403, 406, 108, 109 and 110. Figs. 4a-4c show only details of the operation fields included in the sub-instructions and neither of the operation fields alone can be a sub-instruction because the operation fields do not have a CZ field and CD field. It is respectfully submitted that the disclosure is enabling, as well as the claims. It is therefore respectfully requested that the Examiner withdraws the rejections to claims 1-25 under 35 U.S.C. §112, first paragraph.

Applicants respectfully traverse the Examiner's objection to the drawings. Applicants respectfully bring the Examiner's attention to Fig. 12 as well as page 85, line 10 through page 88, line 17, which clearly shows the various registers. It is therefore respectfully requested that the Examiner withdraws the objection to the drawings.

Claims 1, 14 and 21 claim a data processing device comprising an instruction decoder and an instruction execution unit. The instruction execution unit determines whether or not a predetermined condition is satisfied within a predetermined timing prior to executing the instruction. The prior art does not show, teach or suggest delaying a time for determining a condition as claimed in claims 1, 14 and 21.

Claims 1-25 were rejected under 35 U.S.C. §102(e) as being anticipated by, or in the alternate, under 35 U.S.C. § 103 as being unpatentable over *Holmann et al* (U.S. Patent No. 5,815,698).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §102(e) or under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, it is respectfully requested that the Examiner withdraws the rejections to the claims and allows the claims to issue.

Holmann et al appears to disclose in Fig. 13 a basic format 320 of delayed branch instructions. Delayed branch instruction 320 comprises an opcode 321, a field 322 for designating a delayed value and a field 323 for indicating an offset or an address of a target branch address. (col. 13, lines 54-59) When the instruction decoder 8 in the instruction decode unit 8 recognizes that a decoded instruction is a delayed branch instruction, the instruction decoder unit 2 generates a control signal 11 and transfers it to the memory unit 3. In the memory unit 3, the PC controller 13 stores the decoded instruction into register 13A according to the control signal 11 received from the instruction decoder unit 2. Accordingly, the register 13A stores information indicating the target of a delayed branch instruction. The PC controller 13 stores a PC value related to the time when the branch instruction will be executed into register 13B. When the value of the program counter (PC) in the microprocessor is equal to the value stored in register 13B, the PC controller 13 executes the branch instruction based on the target branch information stored in register 13A. That is, the value designated by the target branch information stored in register 13A is set into the program counter (PC). As a result, when the address of a fetched instructions is equal to the value stored in register 13B, the instruction at the target of a branch is fetched in the following cycles. (col. 14, lines 26-45, emphasis added)

Thus, *Holmann et al* merely discloses a microprocessor which can execute a delayed jump instruction where the field 322 designates the time for executing the branch instruction (i.e., *Holmann et al.* does not delay the time to determine that the jump condition is satisfied but only delays execution of the branch instructions). Nothing in *Holmann et al* shows, teaches or suggests delaying the timing of the determination of a predetermined condition, as claimed in claims 1, 14 and 21. Rather, *Holmann et al* merely discloses that the execution of the instruction is delayed. *Holmann et al* does not disclose delaying of the timing to determine the condition (i.e., an execution condition is not determined at a designated timing).

In reference to Figs. 2a and 2b, when instructions 101 without five bit fields of 103, 104, 402, 405, and 107, or 102 without the bit fields of 403, 406, 108, 109, and 110 and the hatched bit files is applied to the data processing device of other than a VLIW architecture, the scope of claims of the present invention is clearly distinguishable from *Holmann et al*. When the parts of Figs. 2a and 2b are omitted (for explanation purposes only) as above, other figures are understandable when several elements are omitted (for explanation purposes only) as follows. In this case, the scope of claims of the present invention is further distinguishable from *Holmann et al.*

In Figs. 1 and 12, omission of 4, 9, 12, S5, S6, and D3;

In Fig. 3, omission of operation_1 and corresponding raws such as IF, D/A, E/M, and W;

In Fig. 8, omission of I02, I12, I22, I32, I42, I52, and I62;

In Fig. 9, omission of I02, I12, I22, I32, I42, I52, and I62 and corresponding raws such as IF, D/A, E/M, and W;

In Fig. 10, omission of I02, I12, I22, I32, I42, I52, and I62, and I72;

In Fig. 11, omission of I02, I12, I22, I32, I42, I52, and I62, and I72, and corresponding raw such as IF, D/A, E/M, and W.

Since nothing in *Holmann et al* shows, teaches or suggests (a) decoding an instruction in a second period and determining the execution condition in a fourth period which starts after a certain duration of the second period as claimed in claim 1, (b) a register storing a value representing a timing of starting to determine an execution **condition** and an instruction execution unit determining the execution condition in response to an event that the timing is detected based upon the value in the first register, as claimed in claim 14, or (c) a field specifying a timing to start a determination of whether a condition is satisfied as claimed in claim 21, it is respectfully requested that the Examiner withdraws the rejection to claims 1, 14 and 21 under 35 U.S.C. §102(e) or in the alternative under 35 U.S.C. §103.

Claims 2-13, 15-20 and 22-25 depend from claims 1, 14 and 21 and recite additional features. It is respectfully submitted that claims 2-13, 15-20 and 22-25 would not have been anticipated by *Holmann et al* within the meaning of 35 U.S.C. §102(e) or obvious over *Holmann et al.* within the meaning of 35 U.S.C. § 103 at least for the reasons as set forth above and since nothing in the reference shows, teaches or suggests determining an execution condition at the timing designated by a value in a third register as claimed in claim 6. Therefore, it is respectfully requested that the Examiner withdraws the

rejection to claims 2-13, 15-20 and 22-25 under 35 U.S.C. §102(e) or in the alternative under 35 U.S.C. § 103.

Thus, it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested. Should the Examiner find that the application is not now in condition for allowance, it is respectfully requested that the Examiner enters this amendment for purposes of appeal.

If for any reason the Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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